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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,954	02/07/2001	Hideaki Minamide	401073	5794

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EXAMINER	
KISS, ERIC B	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,954	MINAMIDE ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,7-12,14-18,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2* is/are allowed.

6)☒ Claim(s) *5,7-9,11,12,14-16,18,26 and 27* is/are rejected.

7)☒ Claim(s) *10 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060626, 20060725*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20060918*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 26, 2006, has been entered.

Claims 2, 5, 7-12, 14-18, 26, and 27 are pending.

Response to Arguments

2. Applicant's arguments, see pp. 7-9, filed June 26, 2006, with respect to the rejection of claims 2, 10, and 17 under 35 U.S.C. § 103(a) have been fully considered and are persuasive. The rejection of claims 2, 10, and 17 has been withdrawn.

3. Applicant's arguments, see pp. 9-12, filed June 26, 2006, with respect to the rejections of claims 5, 7-9, 11, 12, 14-16, 18, 26, and 27 under 35 U.S.C. §§ 102(b) and 103(a) have been fully considered but they are not persuasive.

In response to applicants arguments regarding claims 5, 7-9, 11, 12, 14-16, 18, 26, and 27, the examiner maintains that [Kim99] describes and clearly illustrates how a ladder logic diagram may be divided into blocks associated with rungs for translation (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks). [Kim99] shows a predetermined rung in a ladder diagram (for example, Fig. 4(a)) and corresponding blocks (for example, Fig. 4(c) and Fig. 5).

Allowable Subject Matter

4. Claim 2 is allowed.

5. Claims 10 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Independent claim 2 and dependent claims 10 and 17 describe a control-program-development supporting apparatus which is used for optimizing a sequential-control program (a ladder logic diagram containing rungs) by: (1) excluding not-cited variables and redundant codes, (2) recombining logical operations, and (3) rearranging codes for locally arranging instructions for a common input or output device, all of these optimizations being carried out by the optimization filtering unit **before** compilation of the sequential control program into a form executable by a programmable controller. The prior art of record fails to expressly teach or fairly suggest these features in the context of the control-program development environments as claimed.

Claim Rejections - 35 USC § 102

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 5, 7-9, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Hyung Seok Kim, et al., "A Translation Method of Ladder Diagram on PLC with Application to a Manufacturing Process," 1999 (hereinafter [Kim99]).

As per claim 5, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of controllable blocks, each block including at least one rung (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks); and a compiler which compiles at least some of the controllable blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] further discloses the programmable controller including a microprocessor having pipeline logic (see, for example, section 3.2 on p. 4; see also Non-Final Rejection (07/26/2005) at 10(b) (noting that the TMS320C40 DSP inherently has pipeline logic and a cache, as described in the data sheet supplied by the examiner)).

As per claim 7, [Kim99] further discloses the control program being a ladder logic diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks, each block including at least one rung (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks) at a predetermined rung in the ladder diagram to generate a program file for every controllable block concerned (see, for example, section 3 on pp. 2-4).

As per claim 8, [Kim99] further discloses the control program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks, each block including at least one rung

(see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks) at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file for every controllable block (see, for example, section 3 on pp. 2-4).

As per claim 9, [Kim99] further discloses the control-program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit extracting at least some rungs including instruction to a common input or output device from the ladder diagram, at least some of the rungs extracted constituting one controllable block, and generating a program file for every block (see, for example, section 3 on pp. 2-4).

As per claim 26, [Kim99] discloses a storing unit which stores the execution codes; a microprocessor which includes pipeline logic (an inherent feature of the TMS320C40 digital signal processor; see Non-Final Rejection (07/26/2005) at 10(b) (noting that the TMS320C40 DSP inherently has pipeline logic and a cache, as described in the data sheet supplied by the examiner)) and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control program into a plurality of controllable blocks, each block including at least one rung (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks); and a compiler which compiles at least some of the controllable blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of *Mastering Excel 97*, 4th ed., 1997, by Thomas Chester and Richard H. Alden (hereinafter [ChA97]).

As per claim 11, in addition to the disclosure applied to claim 5, [Kim99] further discloses a processing-time rough-estimating unit which relates a sample program having a known processing time with the control program corresponding to the execution codes to estimate sequential-processing execution time of a programmable controller (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed; [Kim99] further appears to disclose the use of the TMS320C40 digital signal processor for such a purpose, as disclosed, for example, in section 3.2 on p. 4). [Kim99] further discloses determining and selecting the sample program most similar to the control program to estimate processing time (for example, the time calculation depends on the parameter P_basic, which represents the percentage of basic mnemonics, and is changed according to the application program. This parameter, as reflected in Equation 2, adjusts the specific weighting of known mnemonic execution times from Figure 7, thus adjusting the execution time calculation to better reflect actual execution time). [Kim99] fails to expressly disclose the use of a relating table in implementing such relating. However, the

calculated execution time equation (equation (2) on p. 5) contains indexed values (*e.g.*, T_i, where *i* is an index from 1 to 6) related to the execution times of various ladder diagram mnemonics (see Figure 7). As is well known in the computer programming art, a table is an indexed data structure, allowing data to be retrieved and processed based on a unique index. An example of the use of a table (for example, a spreadsheet) in performing a calculation can be found in [ChA97] (see, for example, the loan calculator described on pp. 114-117). It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to include the use of such a table in the execution time calculation of [Kim99] as tables are well suited to such tasks involving calculations performed on indexed data (see, e.g., [ChA97] at p. 85).

11. Claims 12, 14-16, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of U.S. Patent No. 5,504,902 to McGrath et al.

As per claim 12, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of blocks, each block including at least one rung (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks); a control-program converting unit which converts at least some of the controllable blocks into advanced-language control programs described with a computer-readable advanced language for every controllable block (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the computer-readable advanced programming languages corresponding to every controllable block into codes

directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the "advanced language" being a high-level language. However, McGrath et al. teaches such a conversion from a ladder-based language to a high-level language (see, for example, col. 4, line 59, through col. 5, line 17). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the conversion of [Kim99] to including such a high-level language. One would be motivated to do so to provide an additional means to edit and debug a control program (see, e.g., Figs. 8a through 8c and col. 2, lines 1-13).

As per claims 14-16, see the disclosure applied above to claims 5 and 7-9. For reasons stated above, such claims also would have been obvious.

As per claim 27, [Kim99] discloses a storing unit which stores the execution codes (see, for example, section 3 on pp. 2-4); a microprocessor which includes pipeline logic (see Non-Final Rejection (07/26/2005) at 10(b) (noting that the TMS320C40 DSP inherently has pipeline logic and a cache, as described in the data sheet supplied by the examiner)) and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program, described with a sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control-program into a plurality of blocks, each block including at least one rung (see, for example, section 3 on pp. 2-4, and in particular, the discussion of Fig. 4, describing the translation of ladder diagram blocks); a control-program converting unit which converts at least some of the controllable blocks into advanced-language control programs described with a universal-computer-readable advanced language for every

controllable block (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of universal-computer-readable advanced programming languages corresponding to every controllable block into codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the "advanced language" being a high-level language. However, McGrath et al. teaches such a conversion from a ladder-based language to a high-level language (see, for example, col. 4, line 59, through col. 5, line 17). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the conversion of [Kim99] to including such a high-level language. One would be motivated to do so to provide an additional means to edit and debug a control program (see, e.g., Figs. 8a through 8c and col. 2, lines 1-13).

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of *McGrath et al.*, as applied to claim 12 above, and further in view of [ChA97].

As per claim 18, in addition to the disclosure applied to claim 12, [Kim99] further discloses a processing-time rough-estimating unit which relates a sample program having a known processing time with the control program corresponding to the execution codes to estimate sequential-processing execution time of a programmable controller (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed; [Kim99] further appears to disclose the use of the TMS320C40 digital signal processor for such a purpose, as disclosed, for example, in section 3.2 on p. 4). [Kim99] further discloses determining and selecting the sample program most similar to the control program to estimate processing time (for example, the time

calculation depends on the parameter P_basic, which represents the percentage of basic mnemonics, and is changed according to the application program. This parameter, as reflected in Equation 2, adjusts the specific weighting of known mnemonic execution times from Figure 7, thus adjusting the execution time calculation to better reflect actual execution time). [Kim99] fails to expressly disclose the use of a relating table in implementing such relating. However, the calculated execution time equation (equation (2) on p. 5) contains indexed values (*e.g.*, T_i, where *i* is an index from 1 to 6) related to the execution times of various ladder diagram mnemonics (see Figure 7). As is well known in the computer programming art, a table is an indexed data structure, allowing data to be retrieved and processed based on a unique index. An example of the use of a table (for example, a spreadsheet) in performing a calculation can be found in [ChA97] (see, for example, the loan calculator described on pp. 114-117). It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to include the use of such a table in the execution time calculation of [Kim99] as tables are well suited to such tasks involving calculations performed on indexed data (see, e.g., [ChA97] at p. 85).

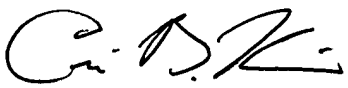
Conclusion

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature should be directed to the TC 2100 Group receptionist: 571-272-2100.



Eric B. Kiss
September 18, 2006